

**In the Claims:**

**Please enter the following amended claims 3, 4, 9 and 12:**

3. (Twice Amended) A memory array comprising:
  - a plurality of floating gate transistors connected in series,
  - each floating gate transistor having formed, in a well of a substrate,
  - a source and a drain region
  - and
  - a channel region separating said source and drain regions,
  - a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant.
4. (Twice Amended) The memory array of claim 3 wherein said dopant concentration region is formed by a tilted ion implantation utilizing as a mask, at least a part of a gate structure of each floating gate transistor.
9. (Twice Amended) A transistor comprising:
  - in a well structure of a substrate, a source and a drain region and a channel region separating said source and said regions, a dopant concentration region displaced about a target region, said target region situated below said channel region, said dopant concentration region extending into said channel region such that said channel region has a non-uniform concentration of dopant.

12. (Once Amended) The transistor of claim 9 wherein said dopant concentration region is provided by a tilted ion implantation utilizing as a mask, at least part of a gate structure of said transistor.